- a capacitor (2C) coupled between a first junction of the bases of said first and second transistors and a second junction of the bases of said third and fourth transistors.

A1 end

9. (amended) Phase shifter in accordance with claim 7, characterized in that said transistors are npn transistors.

10. (amended) Phase shifter in accordance with claim 7, characterized in that said predetermined potential is zero (ground).

11. (amended) Data and clock recovery unit comprising a phase detector (20) which includes a phase shifter in accordance with claim 1.

REMARKS

The foregoing amendments to the claims were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights he may have under the Doctrine of Equivalents. Applicant furthermore

reserves his right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

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APPENDIX

3. (amended) Phase shifter in accordance with claim 1~~ or 2~~, characterized by a first transimpedance converter (12) having its input connected to said input means (IN).

4. (amended) Phase shifter in accordance with ~~at least any one of claims 1 to 3~~claim 1, characterized by

- a second transimpedance converter (14) having its output connected to said first output (OUT+), and
- a third transimpedance converter (15) having its output connected to said second output (OUT).

5. (amended) Phase shifter in accordance with claim 3~~ and/or 4~~, characterized in that the transimpedance converter (12; 14; 15) is a transimpedance amplifier.

6. (amended) Phase shifter in accordance with ~~claims 2 and 4~~claim 2, characterized in that said first and second output buffer means are said second and third transimpedance converters (14, 15), respectively.

7. (amended) Phase shifter in accordance with ~~at least any one of claims 1 to 6~~claim 1,

characterized by at least

- a first transistor (T_1) with its collector connected to its base and its emitter coupled to a predetermined potential,
- second transistor (T_2) with its base connected to the base of said first transistor and its emitter coupled to said predetermined fixed potential, and
- a capacitor (C) coupled between the junction of the bases of said first and second transistor (T_1, T_2) and said predetermined potential.

8. (amended) Phase shifter in accordance with ~~at least any one of claims 1 to 6~~claim 1, provided as a differential phase shifter comprising

- a first input (IN+) for inputting an input signal, and
- a second input (IN-) for inputting an inverse input signal,

characterized by at least

- a first transistor with its collector connected to its base and its emitter coupled to a predetermined potential,

- a second transistor with its base connected to the base of said first transistor and its emitter coupled to said predetermined potential,

- a third transistor with its collector connected to its base and its emitter coupled to a predetermined potential,

- a fourth transistor with its base connected to the base of said third transistor and its collector coupled to said predetermined potential, and

- a capacitor (2C) coupled between a first junction of the bases of said first and second transistors and a second junction of the bases of said third and fourth transistors.

9. (amended) Phase shifter in accordance with claim 7 ~~or 8~~, characterized in that said transistors are npn transistors.

10. (amended) Phase shifter in accordance with ~~at least any one of claims 7 to 9~~claim 7, characterized in that said predetermined potential is zero (ground).

11. (amended) Data and clock recovery unit comprising a phase detector (20) which includes a phase shifter in accordance with ~~at least any one of the preceding claims~~claim 1.